IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
Docket No. 15057US02

In the Application of:

Kimming So, et al.

Serial No.: 10/750,523

Filed: December 31, 2003

For: A MINI-TRANSLATION LOOKASIDE BUFFER FOR USE IN MEMORY TRANSLATION

Examiner: Yaima Campos

Group Art Unit: 2185

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Electronically Filed on April 29, 2008

BRIEF ON APPEAL

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

The Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the final rejection of Claims 12-44 of the present Application. This Brief on Appeal is being filed in response to Appellants' Notice of Appeal filed on January 29, 2008.

REAL PARTY IN INTEREST

The real party in interest is Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 5300 California Avenue, Irvine, CA 92617. Broadcom Corporation is the assignee of the present Application.

RELATED APPEALS AND INTERFERENCES

Not Applicable.

STATUS OF THE CLAIMS

The present Application originally consisted of Claims 1-20. Claims 1-11 have been cancelled and Claims 21-44 have been added. Pending Claims 12-44 stand rejected and are the subject of this appeal. The text of the pending claims and their status is provided in the Claims Appendix.

STATUS OF THE AMENDMENTS

Subsequent to the final rejection mailed on October 29, 2007, the Appellants filed Responses Under 37 C.F.R. § 1.116 on December 15, 2006 and December 19, 2007. As indicated in their respective Advisory Actions dated January 23, 2007 and January 8, 2008, their respective proposed amendments were entered by the Examiner.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 12 is directed to method of improving the performance of address translation in a translation lookaside buffer. The method comprises using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer. The subject matter of Claim 12 is illustratively described in the present Application at, for example, paragraphs [21-22]:

> [21] Aspects of the present invention may be found in a method and system to perform memory address translations to accomplish memory mapping for a control processor (i.e., a CPU) by way of a miniature version of a translation lookaside buffer (TLB). The miniature version of a TLB is termed a mini-TLB. The mini-TLB accomplishes odd/even page frame number translations by way of a single page frame number field instead of a dual page frame number field that is typically used in a TLB. In one embodiment, a mini-TLB facilitates the use of a decreased memory size in comparison to that used by a TLB. The address translation may be accomplished by using an existing control processor instruction set such as that provided by a MIPS control processor instruction set. In addition to using a reduced a TLB of reduced size, the system and method facilitates a more efficient and direct approach in performing virtual to physical memory address translation.
>
> [22] Aspects of the present invention provide performance improvements to one or more control processor virtual to physical memory addressing translation schemes. More specifically, aspects of the present invention obviate mapping virtual addresses into odd and even physical pages, thereby providing an effective way of addressing a translation

> lookaside buffer to facilitate improved CPU processing. A virtual page number of a virtual address to a TLB is mapped to a single page frame number field instead of two page frame number fields. Because TLB lookups are required for every instruction fetch and every load or store instruction, a simplified address translation scheme correlates to decreased lookup times, thereby providing significant improvement to overall control processing performance. For example, each virtual page number (VPN) entry, used by an exemplary MIPS R4000 or MIPS R5000 control processor, is typically associated with two consecutive page frame numbers that are mapped to two different page frame fields (PFN0 and PFN1) within the TLB. For example, two consecutive physical pages of physical memory, one even and one odd, are respectively mapped to two different address sections or fields within a typical TLB. Aspects of the present invention describe how the two page frame number fields (odd and even page frame numbers fields) are consolidated into a single page frame number field of a mini-TLB. A bit from a virtual page number (VPN) of a virtual address to a mini-TLB, such as the VPN's least significant bit (lsb), is used to map odd and even physical pages or page frames into a single page frame number field of the mini-TLB. By utilizing this technique, the mini-TLB utilizes significantly less buffer space.

Claim 16 is directed to a system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers. The subject matter of Claim 16 is illustratively described in the present Application at, for example, paragraphs [21-22]:

> [21] Aspects of the present invention may be found in a method and system to perform memory address translations to accomplish memory mapping for a control processor (i.e., a CPU) by way of a miniature version of a translation lookaside buffer (TLB). The miniature version of

a TLB is termed a mini-TLB. The mini-TLB accomplishes odd/even page frame number translations by way of a single page frame number field instead of a dual page frame number field that is typically used in a TLB. In one embodiment, a mini-TLB facilitates the use of a decreased memory size in comparison to that used by a TLB. The address translation may be accomplished by using an existing control processor instruction set such as that provided by a MIPS control processor instruction set. In addition to using a reduced a TLB of reduced size, the system and method facilitates a more efficient and direct approach in performing virtual to physical memory address translation.

[22] Aspects of the present invention provide performance improvements to one or more control processor virtual to physical memory addressing translation schemes. More specifically, aspects of the present invention obviate mapping virtual addresses into odd and even physical pages, thereby providing an effective way of addressing a translation lookaside buffer to facilitate improved CPU processing. A virtual page number of a virtual address to a TLB is mapped to a single page frame number field instead of two page frame number fields. Because TLB lookups are required for every instruction fetch and every load or store instruction, a simplified address translation scheme correlates to decreased lookup times, thereby providing significant improvement to overall control processing performance. For example, each virtual page number (VPN) entry, used by an exemplary MIPS R4000 or MIPS R5000 control processor, is typically associated with two consecutive page frame numbers that are mapped to two different page frame fields (PFN0 and PFN1) within the TLB. For example, two consecutive physical pages of physical memory, one even and one odd, are respectively mapped to two different address sections or fields within a typical TLB. Aspects of the present invention describe how the two page frame number fields (odd and even page frame numbers fields) are consolidated into a single page frame

> number field of a mini-TLB. A bit from a virtual page number (VPN) of a virtual address to a mini-TLB, such as the VPN's least significant bit (lsb), is used to map odd and even physical pages or page frames into a single page frame number field of the mini-TLB. By utilizing this technique, the mini-TLB utilizes significantly less buffer space.

Claim 18 is directed to a system to provide virtual to physical memory address translation of a translation lookaside buffer. The system comprises a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field. The subject matter of Claim 18 is illustratively described in the present Application at, for example, paragraphs [21-22]:

> [21] Aspects of the present invention may be found in a method and system to perform memory address translations to accomplish memory mapping for a control processor (i.e., a CPU) by way of a miniature version of a translation lookaside buffer (TLB). The miniature version of a TLB is termed a mini-TLB. The mini-TLB accomplishes odd/even page frame number translations by way of a single page frame number field instead of a dual page frame number field that is typically used in a TLB. In one embodiment, a mini-TLB facilitates the use of a decreased memory size in comparison to that used by a TLB. The address translation may be accomplished by using an existing control processor instruction set such as that provided by a MIPS control processor instruction set. In addition to using a reduced a TLB of reduced size, the system and method facilitates a more efficient and direct approach in performing virtual to physical

memory address translation.

[22] Aspects of the present invention provide performance improvements to one or more control processor virtual to physical memory addressing translation schemes. More specifically, aspects of the present invention obviate mapping virtual addresses into odd and even physical pages, thereby providing an effective way of addressing a translation lookaside buffer to facilitate improved CPU processing. A virtual page number of a virtual address to a TLB is mapped to a single page frame number field instead of two page frame number fields. Because TLB lookups are required for every instruction fetch and every load or store instruction, a simplified address translation scheme correlates to decreased lookup times, thereby providing significant improvement to overall control processing performance. For example, each virtual page number (VPN) entry, used by an exemplary MIPS R4000 or MIPS R5000 control processor, is typically associated with two consecutive page frame numbers that are mapped to two different page frame fields (PFN0 and PFN1) within the TLB. For example, two consecutive physical pages of physical memory, one even and one odd, are respectively mapped to two different address sections or fields within a typical TLB. Aspects of the present invention describe how the two page frame number fields (odd and even page frame numbers fields) are consolidated into a single page frame number field of a mini-TLB. A bit from a virtual page number (VPN) of a virtual address to a mini-TLB, such as the VPN's least significant bit (lsb), is used to map odd and even physical pages or page frames into a single page frame number field of the mini-TLB. By utilizing this technique, the mini-TLB utilizes significantly less buffer space.

The invention of Claim 18 is also described in other parts of the Application, such as in the Brief Summary of the Invention, at paragraph [10]:

> [10] Aspects of the invention provide for a method, system and/or apparatus to reduce memory size of a translation lookaside buffer (TLB). Odd and even page frame numbers are stored and accessed as consecutive page frame numbers using a single page frame number field in the mini-TLB. This is accomplished by utilizing a bit obtained from an associated virtual page number of a virtual address. In one embodiment, a bit obtained from a virtual page number, such as the least significant bit of a virtual page number, is used to identify and store even and odd page frame numbers as consecutive page frame numbers using a single page frame number field of the mini-translation lookaside buffer (mini-TLB). In one embodiment, the mini-TLB is configured by way of a control processor instruction set. In one embodiment, the virtual page number of a 4 kilobyte page is defined by bits [31:12] of an exemplary 32 bit virtual address. In one embodiment, a page mask size ranges from 4 kilobytes to 16 megabytes while in another embodiment, the page mask size is 4 kilobytes. In one embodiment, storing and recalling the address translation data of the mini-translation lookaside buffer is facilitated by way of using one or more registers. In one embodiment, the registers comprise a page mask register, an entry Hi register, an entry Lo0 register, and an entry Lo1 register.

Claim 21 is directed to a method which comprises obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for: a) writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame

numbers into said single page frame number field when said bit is a second value, or b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field. The subject matter of Claim 21 is illustratively described in the present Application at, for example, paragraph 22:

> [22] Aspects of the present invention provide performance improvements to one or more control processor virtual to physical memory addressing translation schemes. More specifically, aspects of the present invention obviate mapping virtual addresses into odd and even physical pages, thereby providing an effective way of addressing a translation lookaside buffer to facilitate improved CPU processing. A virtual page number of a virtual address to a TLB is mapped to a single page frame number field instead of two page frame number fields. Because TLB lookups are required for every instruction fetch and every load or store instruction, a simplified address translation scheme correlates to decreased lookup times, thereby providing significant improvement to overall control processing performance. For example, each virtual page number (VPN) entry, used by an exemplary MIPS R4000 or MIPS R5000 control processor, is typically associated with two consecutive page frame numbers that are mapped to two different page frame fields (PFN0 and PFN1) within the TLB. For example, two consecutive physical pages of physical memory, one even and one odd, are respectively mapped to two different address sections or fields within a typical TLB. Aspects of the present invention describe how the two page frame number fields (odd and even page frame numbers fields) are consolidated into a single page frame

> number field of a mini-TLB. A bit from a virtual page number (VPN) of a virtual address to a mini-TLB, such as the VPN's least significant bit (lsb), is used to map odd and even physical pages or page frames into a single page frame number field of the mini-TLB. By utilizing this technique, the mini-TLB utilizes significantly less buffer space.

The invention of Claim 21 is also described in other parts of the Application, such as in paragraph [26] in reference to Figure 3.

> [26] Figure 3 is a relational block diagram illustrating an organizational structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0

> or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or entry the Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304.

The invention of Claim 21 is also described in other parts of the Application, such as at paragraphs [32-33], in reference to Figures 4 and 5, respectively:

> [32] Figure 4 is a relational block diagram illustrating an organizational structure of a mini-TLB system 400 performing a read (TLBR) operation in accordance with an embodiment of the invention. As illustrated in the diagram of Figure 4, the least significant bit (lsb) of a particular VPN is used to determine whether the contents of the page frame number (PFN) is stored in either entry Lo0 or entry Lo1 registers. For example, if the lsb corresponds to the value 0 (signifying an even page), then the contents of the mini-TLB 404 located in the PFN field of a particular page table entry is accessed and written into the entry Lo0 register. However, if the lsb corresponds to the value 1 (signifying an odd page), then the contents of the mini-TLB 404 located in the PFN field of a particular page table entry

is accessed and written into the entry Lo1 register. It is contemplated that these operations may be programmed by using one or more instructions provided by any existing instruction set (i.e., a MIPS instruction set). The contents of the page mask register is stored into the Mask field of the indexed mini-TLB page entry.

[33] Figure 5 is a relational block diagram illustrating an organizational structure of a mini-TLB system 500 performing a write (TLBWI) or random write (TLBWI) operation in accordance with an embodiment of the invention. In this embodiment, a control processor verifies, by performing one or more checks, whether the contents provided by entry Lo0 or entry Lo1 contains a valid PFN. It may perform this check by verifying the contents of the associated VPN stored in the virtual page number field corresponding to a particular page table entry in the mini-TLB 504. For example, the control processor may be programmed to verify the value of the lsb in the entry Hi register. If the value of the lsb in the entry Hi register is 0, the contents of the entry Lo0 register is written into the appropriate PFN field indexed by the mini-TLB page entry. If the value of the lsb in the entry Hi register equals the value 1, the contents of the entry Lo1 register is written into the appropriate PFN field as indexed by the mini-TLB page table entry. Thereafter, the contents of the page mask register is stored into the Mask field of the indexed mini-TLB page entry.

Claim 29 is directed to a method of performing a write operation using a translation lookaside buffer. The method comprises using a bit of a virtual page number, said virtual page number stored in a data register; assessing whether a value of said bit of a virtual page number is 0 or 1; writing a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if

said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer. The subject matter of Claim 29 is illustratively described in the present Application at, for example, paragraph [26], referring to Figure 3:

> [26] Figure 3 is a relational block diagram illustrating an organizational structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0

> or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or entry the Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304.

The invention of Claim 29 is also described in other parts of the Application, such as at paragraph [29], in reference to Figure 3:

> [29] TLBWI (TLB Write) - writes contents of either entry Lo0 or entry Lo1 registers into a page frame number (PFN) field of a corresponding mini-TLB entry (or page table entry). The mini-TLB entry is identified by contents provided by the Index register. When writing to the mini-TLB, only one of the entry Lo registers (either entry Lo0 or entry Lo1) has valid contents. The entry Lo register with valid contents is written into the PFN field of the mini-TLB.

Furthermore, the subject matter of Claim 29 is described in the present Application, for example, at paragraph [33], referring to Figure 5:

[33] Figure 5 is a relational block diagram illustrating an organizational structure of a mini-TLB system 500 performing a write (TLBWI) or random write (TLBWI) operation in accordance with an embodiment of the invention. In this embodiment, a control processor verifies, by performing one or more checks, whether the contents provided by entry Lo0 or entry Lo1 contains a valid PFN. It may perform this check by verifying the contents of the associated VPN stored in the virtual page number field corresponding to a particular page table entry in the mini-TLB 504. For example, the control processor may be programmed to verify the value of the lsb in the entry Hi register. If the value of the lsb in the entry Hi register is 0, the contents of the entry Lo0 register is written into the appropriate PFN field indexed by the mini-TLB page entry. If the value of the lsb in the entry Hi register equals the value 1, the contents of the entry Lo1 register is written into the appropriate PFN field as indexed by the mini-TLB page table entry. Thereafter, the contents of the page mask register is stored into the Mask field of the indexed mini-TLB page entry.

Claim 32 is directed to a method of performing a read operation using a translation lookaside buffer. The method comprises using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer; assessing whether a value of a bit of a virtual page number is 0 or 1; reading a page frame number stored in a page frame number field of an indexed entry of said translation lookaside buffer; storing said page frame number into a first register if said value is 0; and storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer. The subject matter of Claim 32 is illustratively described in the present Application at, for example, paragraph 26, referring to Figure 3:

[26] Figure 3 is a relational block diagram illustrating an organizational

structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry

> Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or entry the Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304.

The invention of Claim 32 is also described in other parts of the Application, such as at paragraph [28], in reference to Figure 3:

> [28] TLBR (TLB Read) - reads contents from a page frame number (PFN) field of a mini-TLB entry (or page table entry) and transfers the contents into entry Lo0 or entry Lo1 registers. The mini-TLB entry is identified by contents of the Index register. When reading from the mini-TLB, only one of the entry Lo registers (either entry Lo0 or entry Lo1) has valid contents.

The invention of Claim 32 is also described in other parts of the Application, such as at paragraph [32] in reference to Figure 4:

> [32] Figure 4 is a relational block diagram illustrating an organizational structure of a mini-TLB system 400 performing a read (TLBR) operation in accordance with an embodiment of the invention. As illustrated in the diagram of Figure 4, the least significant bit (lsb) of a particular VPN is used to determine whether the contents of the page frame number (PFN) is stored in either entry Lo0 or entry Lo1 registers. For example, if the lsb corresponds to the value 0 (signifying an even page), then the contents of the mini-TLB 404 located in the PFN field of a particular page table entry is accessed and written into the entry Lo0 register. However, if the lsb corresponds to the value 1 (signifying an odd page), then the contents of the mini-TLB 404 located in the PFN field of a particular page table entry

> is accessed and written into the entry Lo1 register. It is contemplated that these operations may be programmed by using one or more instructions provided by any existing instruction set (i.e., a MIPS instruction set). The contents of the page mask register is stored into the Mask field of the indexed mini-TLB page entry.

Claim 34 is directed to a method of probing for a particular virtual page number of an entry in a translation lookaside buffer. The method comprises using a virtual page number stored in a first register; comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register. The subject matter of Claim 34 is illustratively described in the present Application at, for example, paragraph 26, referring to Figure 3:

> [26] Figure 3 is a relational block diagram illustrating an organizational structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the

> embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or entry the Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304.

The invention of Claim 34 is also described in other parts of the Application, such as at paragraph [31], in reference to Figure 3:

> [31] TLBP (TLB probe) – probes or searches the virtual page number field of the TLB for a particular virtual page number as defined by the

> contents in the entry Hi register. Writes the page table entry number or location of the virtual page number into the Index register. One or more bit(s) in the Index register indicates the result of the probe or search.

The invention of Claim 34 is also described in other parts of the Application, such as at paragraph [34] in reference to Figure 6:

> [34] Figure 6 is a relational block diagram illustrating an organizational structure of a mini-TLB system 600 performing a probe or search (TLBP) operation in accordance with an embodiment of the invention. The probe operation is used to perform a search of a particular VPN in the mini-TLB 604. As shown in Figure 6, one or more VPN fields are accessed by the entry Hi register 608 in order to locate the corresponding index entry in the mini-TLB 604. Should a match occur, the corresponding entry identification number is written into one or more least significant bit(s) (lsbs) of the index register 612. The most significant bit (msb) of the index register 612 is used to indicate whether the probe or search resulted in a hit or miss.

Claim 35 is directed to a translation lookaside buffer system. The system comprises a translation lookaside buffer; a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field; a second register used for storing a page size of said entry; a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit; a fourth register used for storing an even page frame number; and a fifth register used for storing an odd page frame number, said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said

translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or said odd page frame number is to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer. The subject matter of Claim 35 is illustratively described in the present Application at, for example, paragraph [26], referring to Figure 3:

> [26] Figure 3 is a relational block diagram illustrating an organizational structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment

> illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or entry the Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304.

The invention of Claim 35 is also described in other parts of the Application, such as at the Brief Summary of the Invention, and at paragraph [21], for example:

> [21] Aspects of the present invention may be found in a method and system to perform memory address translations to accomplish memory mapping for a control processor (i.e., a CPU) by way of a miniature version of a translation lookaside buffer (TLB). The miniature version of a TLB is termed a mini-TLB. The mini-TLB accomplishes odd/even page frame number translations by way of a single page frame number field instead of a dual page frame number field that is typically used in a TLB. In one embodiment, a mini-TLB facilitates the use of a decreased memory size in comparison to that used by a TLB. The address translation may be accomplished by using an existing control processor instruction set such as

> that provided by a MIPS control processor instruction set. In addition to using a reduced a TLB of reduced size, the system and method facilitates a more efficient and direct approach in performing virtual to physical memory address translation.

Claim 41 is directed to a reduced size translation lookaside buffer. The buffer comprises a virtual page number field used to store a virtual page number; a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number. The subject matter of Claim 41 is illustratively described in the present Application at, for example, paragraphs [21-22]:

> [21] Aspects of the present invention may be found in a method and system to perform memory address translations to accomplish memory mapping for a control processor (i.e., a CPU) by way of a miniature version of a translation lookaside buffer (TLB). The miniature version of a TLB is termed a mini-TLB. The mini-TLB accomplishes odd/even page frame number translations by way of a single page frame number field instead of a dual page frame number field that is typically used in a TLB. In one embodiment, a mini-TLB facilitates the use of a decreased memory size in comparison to that used by a TLB. The address translation may be accomplished by using an existing control processor instruction set such as that provided by a MIPS control processor instruction set. In addition to using a reduced a TLB of reduced size, the system and method facilitates a more efficient and direct approach in performing virtual to physical memory address translation.
>
> [22] Aspects of the present invention provide performance improvements to one or more control processor virtual to physical memory addressing translation schemes. More specifically, aspects of the present

invention obviate mapping virtual addresses into odd and even physical pages, thereby providing an effective way of addressing a translation lookaside buffer to facilitate improved CPU processing. A virtual page number of a virtual address to a TLB is mapped to a single page frame number field instead of two page frame number fields. Because TLB lookups are required for every instruction fetch and every load or store instruction, a simplified address translation scheme correlates to decreased lookup times, thereby providing significant improvement to overall control processing performance. For example, each virtual page number (VPN) entry, used by an exemplary MIPS R4000 or MIPS R5000 control processor, is typically associated with two consecutive page frame numbers that are mapped to two different page frame fields (PFN0 and PFN1) within the TLB. For example, two consecutive physical pages of physical memory, one even and one odd, are respectively mapped to two different address sections or fields within a typical TLB. Aspects of the present invention describe how the two page frame number fields (odd and even page frame numbers fields) are consolidated into a single page frame number field of a mini-TLB. A bit from a virtual page number (VPN) of a virtual address to a mini-TLB, such as the VPN's least significant bit (lsb), is used to map odd and even physical pages or page frames into a single page frame number field of the mini-TLB. By utilizing this technique, the mini-TLB utilizes significantly less buffer space.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 12-23, 25, 29-34, and 41-43 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hinton et al. (U.S. Patent No. 5,500,948) (hereinafter, Hinton).

II. Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinton.

III. Claims 26 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinton in view of Bryg et al. (U.S. Patent No. 6,430,670) (hereinafter, Bryg).

IV. Claims 27-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinton in view of Riedlinger et al. (U.S. Patent No. 6,446,187) (hereinafter, Riedlinger).

V. Claims 35-38 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter, AAPA) in view of Hinton.

VI. Claim 39 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Hinton as applied to Claim 38 above, and further in view of Bryg.

ARGUMENT

RESPONSE TO ADVISORY ACTION

In the Advisory Action, the Examiner has made an attempt to respond to pages 8-13 of the response dated December 19, 2007; however, it appears that the Examiner has not considered the Appellants' remarks of this response found on pages 14-45. In responding to the Examiner's remarks throughout the prosecution of the present Application, the Appellants believe that many of the Examiner's remarks repetitively reference irrelevant portions of Hinton without showing a teaching of the elements of a claim.

In response to the Examiner's "First Point of Argument," in the Advisory Action dated January 8, 2008 (hereinafter, Advisory Action), the Appellants respectfully submit that while the Examiner may have "cited specific portions from the prior art of record," the Examiner does not show how these "specific portions" teach what is recited in the pending claims. Therefore, the Examiner has not shown a teaching of each and every element and/or feature recited in the pending claims. For example, in the response dated December 19, 2007, the Appellants had stated the following:

> For example, the Examiner alleges that she shows a teaching by referencing one or more large sections of text in a cited reference without specifically pointing out or logically explaining how each element or feature is taught using the cited references. Applicants would appreciate it if the Examiner would provide the specific words or phrases within the cited references which may be used to teach an element and/or feature of a claim. Furthermore, the Applicants believe that the Examiner has not responded to Applicants' arguments made in the Response dated August

> 15, 2007 since she restates what was previously stated in the Office Action dated May 16, 2007. Also, it appears the Examiner replicates arguments to various claims without providing a specific response to a claim.

Thus, the Examiner has not clearly shown a teaching of what is recited in the pending claims. Therefore, Appellants believe that the pending claims should be allowed.

With respect to Examiner's "Second Point of Argument" in the Advisory Action, Appellants had thoroughly explained how Hinton does not teach what is recited in Claims 29, 32, and 35. Appellants respectfully submit that a small or reduced size translation TWB (translation write buffer) does not teach methods for reducing the size of a translation buffer, as recited in Claims 29, 32, and 35. (In other words, a small buffer does not teach a method that reduces the size of a buffer.) For example, Hinton does not teach "a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claims 29 and 32. Without disclosing any method for reducing memory size, Hinton simply uses a bit to toggle (or select) between two different sets of physical registers (or memory banks), as shown in Figure 3 of Hinton. Therefore, Hinton does not teach what is recited in Claims 29, 32, and 35. Previously, the Appellants had stated in the response dated December 19, 2007:

> As was stated in the interview with the Applicants' representative on January 18, 2007, the Examiner had indicated that the feature "reducing the size of a translation lookaside buffer" had not been given patentable weight since it was recited in the preamble of Claim 1. Therefore, in the request for continued examination (RCE), the Applicants incorporated this patentable feature into Claims 29, 32, and 35 seeking allowance of these claims. However, to the Applicants' disbelief, the Examiner has

> subsequently rejected Claims 29, 32, and 35 by providing flawed reasoning in the Office Actions. For example, the Examiner has repeatedly referenced physical register 0 (element 106) and physical register 1 (element 104), at Col. 6, lines 55-58, and at Figure 3, of Hinton, in her attempt to show a teaching of "reducing the size of a translation lookaside buffer." However, this passage or any other passage in Hinton, does not teach any method or system that reduces the size of a buffer, as recited in several of the pending claims. Hinton merely uses a bit to select from two different registers (i.e., physical register 0 (element 106) and physical register 1 (element 104)) in a buffer (i.e., Hinton's translation write buffer (TWB)), which does not disclose any reduction in memory size in comparison to what is recited in Claims 29, 32, and 35, for example. Therefore, Hinton does not teach or disclose a method or system that reduces the size of a translation lookaside buffer. Therefore, the Examiner has not demonstrated a teaching of at least this patentable feature recited in Claims 29, 32, and 35. Applicants request allowance of Claims 29, 32, and 35 along with their corresponding dependent claims.

Thus, it appears that the Examiner has disregarded Appellants' reasoning. Therefore, the Appellants respectfully request the Board to consider Appellants' argument for this issue.

With respect to Examiner's "Third Point of Argument" in the Advisory Action, it appears that the Examiner has mischaracterized what is disclosed in Hinton, in an attempt to show a teaching of Claim 21. As referenced by the Examiner and disclosed in Hinton, at col. 7, lines 19-20, "the control logic selects one of these register's hit signals." In the Advisory Action, the Examiner interprets this as "comprises reading from the TWB; which corresponds to Appellant's claimed TLB." Appellants respectfully disagree with this interpretation and believe that the Examiner has mischaracterized what is disclosed in Hinton. Hinton does not disclose "*reading* from the TWB," as alleged by the Examiner.

Appellants respectfully submit that the act of selecting a register's hit signals does not correspond to reading from a buffer (TWB). The Appellants had previously presented the following argument in the response dated December 19, 2007:

> The Examiner wishes to use a TWB (translation write buffer) in Hinton to teach a TLB (translation lookaside buffer) providing write and read functionality (emphasis denoted in italics), in the manner recited in one or more method and system claims (e.g., independent Claims 18, 21, 32, 35). The Applicants have repeatedly stated that the cited reference (Hinton) does not disclose a TLB providing read functionality as recited in these claims since Hinton does not teach or disclose each and every element that is recited in these claims. The Examiner fails to show a teaching of how Hinton's TWB provides read functionality as recited in these claims. The Examiner's complete response, as found on page 22 of the last Office Action is to simply state that "Hinton expressly discloses a ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5)]; therefore, TWB is a TLB of reduced/mini size." Furthermore, the Applicants have examined Cols. 5-6, lines 62-67 and 1-5, but have not found any disclosure of the read functionality recited in Claims 21, 32, and 35, for example. For example, the Applicants request that the Examiner specifically point how each and every element of "b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field" is taught or disclosed by Examiner's cited reference (i.e., Hinton). Applicants believe that the Examiner has failed to address Applicants' arguments. Applicants request

> that the Examiner specifically point out (using specific and direct evidence from the reference, without large portions of text) how each and every element is taught by Hinton.

As was stated in the above passage, the Appellants requested that the Examiner specifically point how each and every element of "b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field" is taught or disclosed by Examiner's cited reference (i.e., Hinton). Appellants believe that the Examiner has not addressed Appellants' request and that the Examiner has not specifically shown (using specific evidence from the reference, and by providing a logical explanation) how each and every element is taught by Hinton.

With respect to Examiner's "Fourth Point of Argument" in the Advisory Action, the Examiner attempts to show a teaching of "consolidating even and odd page frame numbers into a single page frame number field," as recited in Claim 12. The Examiner alleges that Hinton teaches this at various paragraphs: col. 5-6, lines 62-67 and 1-5; at col. 2-3, lines 64-67 and 1-5; col. 1-2, lines 64-67 and 1-29; col. 6, lines 37-63; Figure 3; col. 7, lines 5-14; and col. 7, line 54 – col. 8, line 45. Without providing a rational explanation, the Examiner concludes by stating: "Therefore, even logical and physical address set is read from/written to TWB and odd logical and physical address set are read from/written to TWB. Therefore, Hinton discloses writing and reading even and odd page

frame numbers into a single page frame number field." Appellants do not remotely see how "even logical and physical address set is read from/written to TWB and odd logical and physical address set are read from/written to TWB" teaches "consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer."

Furthermore, the Examiner provides an interpretation by stating:

> For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant][sic].

Thus, by providing the foregoing interpretation, the Examiner admits that two separate fields are used: one field in physical register 0 and one field in physical register 1. Consequently, *two fields* (one field in physical register 0, another field in physical register 1) do not teach "a *single* page frame number *field*," as recited in Claim 12. Therefore, for at least these reasons, the Examiner has not shown a teaching of what is recited in Claim 12.

With respect to Examiner's "Fifth Point of Argument" in the Advisory Action, the Examiner restates Appellants' argument presented in the response dated December 19, 2007:

> Regarding the following remark:
>
> The Examiner states that Hinton discloses "reading from on(e) [sic] of the registers of (Hinton's) TWB, as claimed." However, the Examiner is incorrect, since the claimed invention does not recite registers within a buffer. For example, Hinton does not teach the "first storage register" and "second storage register," as recited in Claim 18 because Hinton's registers are contained within a buffer (Le., the TWB). Furthermore, the Examiner is requested to review the supporting specification, at Figure 3, which clearly illustrates the relationship of the claimed translation lookaside buffer (TLB) and the registers. As illustrated in Figure 3, the TLB does not comprise the registers. Hence, the Examiner does not show a teaching of what is recited in at least Claim 18, for example. Likewise, the Examiner does not show a teaching of the pending claims. Therefore, the pending claims should be passed to allowance.

Furthermore, the Examiner responds to Appellants' argument by stating that "The Examiner would like to point out that claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]) and claim 18, for example, does not recite any limitations regarding the location of a first register and a second register." Appellants respectfully submit that Claim 18 recites a system comprising three separate elements: a) translation lookaside buffer; b) a first register; and c) a second register. Therefore, for at least this reason, Claim 18 does not disclose a translation lookaside buffer comprising a first register and a second register. Therefore,

the Examiner has not shown a teaching of what is recited in Claim 18. Furthermore, a claim should be interpreted in light of what is disclosed in the specification. As stated in the MPEP, at § 2111, "The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "*in light of the specification* as it would be interpreted by one of ordinary skill in the art." In light of the specification, Figure 3 of the present Application, for example, clearly illustrates that the registers are not resident within a TLB (translation lookaside buffer). Thus, the Examiner has not shown a teaching of what is recited in Claim 18.

With respect to Examiner's "Sixth Point of Argument" in the Advisory Action, the Appellants do not see how a logical address teaches "a virtual page number stored in a first register," as recited in Claim 34. Appellants respectfully submit that Hinton does not disclose "teaches a virtual page number stored in a first register." Thus, the Examiner has not shown a teaching of Claim 34.

I. REJECTION OF CLAIMS 12-23, 25, 29-34, AND 41-43 UNDER U.S.C. 102(b) BY HINTON

A. Independent Claim 12

Claim 12 is directed to:

12. A method of improving the performance of address translation in a translation lookaside buffer comprising:

using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and

consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer.

The Examiner has rejected Claim 12 under 35 U.S.C. § 102(b) as being anticipated by Hinton. The Examiner alleges that Hinton, at Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3, teaches the second clause of Claim 12. Contrary to what the Examiner alleges, nowhere in Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3, as referenced by the Examiner, is there a teaching of "consolidating even and odd page frame numbers into *a single page frame number field*," as recited in Claim 12. Contrary to what the Examiner attempts to teach, Col. 6, lines 37-63 and Fig. 3 of Hinton, discloses *two* distinct and separate registers for storing "physical addresses." Thus, there is no reduction in memory provided by Hinton's invention. The Appellants request the Board to refer to Col. 6, lines 54-59 of Hinton which states the following:

> The physical registers (104, 106) provide stored-physical addresses to the MUX (100). Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one.

As may be easily seen from the above passage from Hinton, Hinton's physical register 104 is used to store odd numbered pages while Hinton's physical register 106 is used to store even numbered pages. Thus, Hinton utilizes two separate memories to store even and odd pages; as a consequence, the method provided by Hinton provides *no* reduction in memory size. Thus, Hinton does not provide any disclosure of "consolidating even

and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in independent Claim 12. For each of these reasons, the Appellants maintain that the Examiner has not shown a teaching of what is recited in independent Claim 12. Therefore, the Appellants respectfully submit that Claim 12 is in condition for allowance.

Furthermore, the Appellants also request the Board to refer to Appellants' preceding argument with respect to Examiner's "Fourth Point of Argument" of the Advisory Action.

In addition, the Appellants believe that the Examiner has improperly characterized and/or interpreted what is disclosed in Hinton. For example, at the first paragraph of page 4 of the Office Action dated 5/16/07, the Examiner states that **"Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer)."** The Appellants respectfully submit that an "even or an odd logical and physical address set" does not teach a "page frame number field," as recited in Claim 12. Nowhere does Claim 12 recite anything about *an even or odd logical and physical address set*. Thus, for this reason alone, the Examiner has not shown a teaching of what is recited in Claim 12. Furthermore, Hinton does not disclose anything about a page frame number or page frame number field as recited in Claim 12. Thus, for each of these reasons alone, Hinton does not teach what is recited in Claim 12; as a consequence, Claim 12 contains patentable subject matter and should be allowed.

In addition, as the Appellants had stated in the Preliminary Amendment and Request for Continued Examination dated February 22, 2007, Hinton's translation write buffer (TWB) does not teach a translation lookaside buffer (TLB) recited in Claim 12. Furthermore, Hinton's TWB comprises elements that are functionally different from Appellants' claimed invention. For example, Hinton's TWB comprises two sets of physical registers and logical registers (as illustrated in Hinton, at Figure 3). A translation write buffer does not teach a "translation lookaside buffer," as recited in Claim 12, and as interpreted in light of the specification (per MPEP §2111). Therefore, for each of these reasons, Appellants respectfully submit that Hinton does not teach the method recited in Claim 12. Therefore, the Appellants respectfully request allowance of the patentable subject matter recited in Claim 12.

Furthermore, the Examiner has failed to provide a logical explanation as to how Hinton, at Col. 7, line 54 – Col. 8, line 45, may be used to show a teaching of Claim 12. In an attempt to show a teaching, the Examiner references one or more large sections of text in a cited reference without specifically pointing out or logically explaining how a word or phrase within a large section of text teaches what is recited in a claim. The Appellants respectfully submit that the Examiner has not made an attempt to clearly and specifically point out how the verbiage of Hinton, at Col. 7, line 54 – Col. 8, line 45, for example, teaches the elements and/or features recited in Claim 12. Furthermore, the Examiner has failed to provide any sort of argument that addresses the newly presented elements and/or features that were incorporated into Claim 12. For example, the Examiner has failed to show a teaching of "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd." Therefore, for at least

these reasons, the Appellants respectfully submit that independent Claim 12 contains patentable subject matter, and that these claims should be passed to allowance. Furthermore, since for at least the reason that Claims 13-15 depend on Claim 12, Claims 13-15 should be allowed as well.

B. Dependent Claim 15

Claim 15 is directed to:

15. The method of Claim 12 wherein said consolidating even and odd page frame number fields into said single page frame number field implements a translation lookaside buffer of reduced size.

The Examiner has referenced Hinton, physical register 0 (element 106) and physical register 1 (element 104), at Figure 3, in her attempt to show a teaching of implementing a translation lookaside buffer of reduced size. However, the Appellants do not see any disclosure by Hinton, of "implement[ing] a translation lookaside buffer of reduced size," since Hinton discloses a bit used to select from two different registers (i.e., physical register 0 (element 106) and physical register 1 (element 104)) located within a buffer (Hinton's translation write buffer (TWB)). Thus, Hinton does not teach or disclose a method or system that reduces the size of a buffer. Therefore, the Appellants respectfully submit that the Examiner does not show a teaching of what is recited in Claim 15. Since Claim 15 recites "consolidating even and odd page frame number fields using a single page frame number field [to implement] a translation lookaside buffer of reduced size" (compared with using two page frame number fields, which would take up

more memory space), the Examiner's reference to a physical register 0 (element 106) and a physical register 1 (element 104) at Col. 6, lines 55-58, and at Figure 3 of Hinton does not teach what is recited in Claim 15. Therefore, the Examiner has not shown a teaching of Claim 15. Consequently, the Appellants request allowance of Claim 15.

C. Independent Claim 16

Claim 16 is directed to:

16. A system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers.

The Examiner has rejected Claim 16 under 35 U.S.C. § 102(b) as being anticipated by Hinton. The Examiner alleges that Hinton, at Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3, teaches Claim 16. Contrary to what the Examiner alleges, nowhere in Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3 is there a teaching of "a buffer that uses a single page frame number field for storing odd/even page frame numbers," as recited in Claim 16. Contrary to what the Office Action attempts to teach, Col. 6, lines 37-63 and Fig. 3 of Hinton, discloses *two* distinct and separate registers for storing "physical addresses." Thus, there is no reduction in memory provided by Hinton's invention. The Appellants request the Examiner to refer to Col. 6, lines 54-59 of Hinton which states the following:

> The physical registers (104, 106) provide stored-physical addresses to the MUX (100). Registers (106) marked "0" are for even-numbered

> 4KB pages, addresses for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one.

As may be easily seen from the above passage from Hinton, Hinton's physical register 104 is used to store odd numbered pages while Hinton's physical register 106 is used to store even numbered pages. Thus, Hinton utilizes two separate memories to store even and odd pages; as a consequence, there is *no* reduction in memory provided by Hinton. Thus, Hinton does not provide any disclosure of "a single page frame number field for storing odd/even page frame numbers," as recited in Claim 16. For each of these reasons, the Appellants maintain that the Examiner has not shown a teaching of what is recited in independent Claim 16. Therefore, the Appellants respectfully submit that Claim 16 is in condition for allowance.

Furthermore, the Appellants believe that the Examiner has improperly characterized and/or interpreted what is disclosed in Hinton. For example, at the first paragraph of page 4 of the Office Action dated 5/16/07, the Examiner states that "**Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer).**" First of all, nowhere does Claim 16 recite anything about *an even or odd logical and physical address set*. Thus, for this reason alone, the Appellants believe that the Examiner has not shown a teaching of what is recited in Claim 16. Secondly, Hinton does not disclose anything about a page frame number or page frame number field as recited in Claim 16. Thus, for each of these reasons alone, Hinton does not teach what is

recited in Claim 16; as a consequence, Claim 16 contains patentable subject matter that should be allowed.

Furthermore, the Examiner has failed to provide a logical explanation as to how Hinton, at Col. 7, line 54 – Col. 8, line 45, may be used to show a teaching of Claim 16. In an attempt to show a teaching, the Examiner has referenced one or more large sections of text in Hinton without specifically pointing out or logically explaining how a large section of text teaches what is recited in this claim. The Appellants respectfully submit that the Examiner has not been able to logically point out how the verbiage of Hinton, at Col. 7, line 54 – Col. 8, line 45, teaches what is recited in Claim 16. Therefore, for at least these reasons, the Appellants respectfully submit that independent Claim 16 contains patentable subject matter, and that these claims should be passed to allowance. Furthermore, since for at least the reason that Claim 17 depends on Claim 16, Claim 17 should be allowed as well.

D. Dependent Claim 17

Claim 17 is directed to:

17. (Original) The system of Claim 16 wherein said buffer comprises a translation lookaside buffer of reduced size.

The Examiner has referenced Hinton, physical register 0 (element 106) and physical register 1 (element 104), at Figure 3, in her attempt to show a teaching of implementing a translation lookaside buffer of reduced size. However, the Appellants do not see any disclosure by Hinton, of "implement[ing] a translation lookaside buffer of reduced size," since Hinton discloses a bit used to select from two different registers (i.e.,

physical register 0 (element 106) and physical register 1 (element 104)) located within a buffer (Hinton's translation write buffer (TWB)). Thus, Hinton does not teach or disclose a method or system that reduces the size of a buffer. Since Claim 17 recites "wherein said buffer comprises a translation lookaside buffer of reduced size" (compared with using two page frame number fields, which would take up more memory space), the Examiner's reference to a physical register 0 (element 106) and a physical register 1 (element 104) at Col. 6, lines 55-58, and at Figure 3 of Hinton does not teach what is recited in Claim 17. Therefore, the Examiner has not shown a teaching of Claim 17. Consequently, the Appellants request allowance of Claim 17.

E. Independent Claim 18

Claim 18 is directed to:

18. A system to provide virtual to physical memory address translation of a translation lookaside buffer comprising:

a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer;

a first register for mapping an even page frame number to said single page frame number field; and

a second register for mapping an odd page frame number to said single page frame number field.

The Examiner has rejected Claim 18 under 35 U.S.C. § 102(b) as being anticipated by Hinton. The Examiner alleges that Hinton, at Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3, teaches the first clause of Claim 18. Contrary to what the

Examiner alleges, nowhere in Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3, as referenced by the Examiner, is there a teaching of "using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer" as recited in Claim 18. Contrary to what the Office Action attempts to teach, Col. 6, lines 37-63 and Fig. 3 of Hinton, discloses *two* distinct and separate registers for storing "physical addresses." Thus, there is no reduction in memory provided by Hinton's invention. The Appellants request the Examiner to refer to Col. 6, lines 54-59 of Hinton which states the following:

> The physical registers (104, 106) provide stored-physical addresses to the MUX (100). Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers ((104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one.

As may be easily seen from the above passage from Hinton, Hinton's physical register 104 is used to store odd numbered pages while Hinton's physical register 106 is used to store even numbered pages. Thus, Hinton does not disclose "a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field," as recited in Claim 18. Instead, Hinton utilizes two separate memories to store even and odd pages. Thus, Hinton does not provide any disclosure of "using a bit of a virtual page

number of a virtual address for reading and writing odd and even page frame numbers using a *single* page frame number *field* of said translation lookaside buffer," as recited in Claim 18. For these reasons, the Appellants maintain that the Examiner has not shown a teaching of what is recited in independent Claim 18. Therefore, the Appellants respectfully submit that Claim 18 is in condition for allowance.

Appellants believe that the Examiner has improperly characterized and/or interpreted what is disclosed in Hinton. For example, at the first paragraph of page 4 of the Office Action dated 5/16/07, the Examiner states that **"Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer)."** First of all, based on what the Examiner has stated, nowhere does Claim 18 recite anything about *an even or odd logical and physical address set.* Thus, for this reason alone, the Examiner has not shown a teaching of what is recited in Claim 18. The Appellants respectfully submit that "an even or an odd logical and physical address set" does not teach a "page frame number field" as recited in Claim 18. Secondly, it appears that the Examiner wishes to use Hinton, at col. 7, lines 11-14, when she states that the phrase "is loaded" maps to "comprises reading or writing." The Appellants respectfully submit that what Hinton states as "one set (even or odd) of the TWB registers is loaded with the logical and physical addresses" (per Hinton, at col. 7, lines 11-14) does not teach "reading and writing odd and even page frame numbers using a single page frame number field," as recited in Claim 18. Thirdly, Hinton does not disclose anything about a page frame number or page frame number field as recited in Claim 18. Thus, for each of these

reasons, Hinton does not teach what is recited in Claim 18; as a consequence, Claim 18 contains patentable subject matter and should be allowed. The Examiner interprets the term "loaded" to mean "reading or writing" in an attempt to teach a translation lookaside buffer (TLB) recited in Claim 18. Appellants respectfully disagree that the term "loaded" is equivalent to the term "reading or writing." Therefore, the Appellants respectfully submit that for this reason alone, the Examiner has not shown a teaching of what is recited in Claim 18. Therefore, for each of the foregoing reasons, the Office Action does not show a teaching of what is recited in Claim 18.

Furthermore, Appellants had previously indicated in the Preliminary Amendment and Request for Continued Examination dated February 22, 2007, that Hinton's translation write buffer (TWB) does not teach a translation lookaside buffer (TLB) that is recited in Claim 18. Hinton's TWB comprises elements that are functionally different from Appellants' claimed invention. For example, Hinton's TWB comprises two sets of physical registers and logical registers. Hinton's TWB is different from the system recited in Claim 18 since the system comprises a TLB, first and second registers. Further, Hinton's TWB does not teach the TLB recited in Claim 18. Functionally, Hinton's TWB performs write operations only; and as a consequence, it does not teach the "translation lookaside buffer (TLB) using a bit of a virtual page umber of a virtual address for reading and writing odd and even page frame numbers," as recited in Claim 18. Therefore, for each of these reasons, Appellants respectfully submit that Hinton does not teach the system recited in Claim 18. Therefore, the Appellants respectfully request allowance of the patentable subject matter recited in Claim 18.

In addition, the Examiner has failed to provide a logical explanation as to how Hinton, at Col. 7, line 54 – Col. 8, line 45, may be used to show a teaching of Claim 18. In an attempt to show a teaching, the Examiner references one or more large sections of text in a cited reference without logically explaining how the large sections of text teaches what is recited in this claim. For example, the Appellants respectfully submit that the Examiner has not made an attempt to clearly show how the verbiage of Hinton, at Col. 7, line 54 – Col. 8, line 45, teaches each and every element and/or feature recited in Claim 18. Furthermore, the Appellants respectfully submit that the Examiner has not provided a new argument that addresses the newly presented elements and/or features incorporated into Claim 18 (i.e., presented in the response to office action dated August 15, 2007). For example, the Examiner has not shown a teaching of "a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field," as recited in Claim 18. Therefore, for at least these reasons, the Appellants respectfully submit that independent Claim 18 contains patentable subject matter that should be passed to allowance. Appellants respectfully request allowance of independent Claim 18. Furthermore, for at least the reason that Claims 19-20 depend on Claim 18, Claims 19-20 should be allowed as well.

F. Dependent Claim 19

Claim 19 is directed to:

19. The system of Claim 18 wherein using a single page frame number field implements a reduced size of said translation lookaside buffer.

The Examiner has referenced Hinton, physical register 0 (element 106) and physical register 1 (element 104), at Figure 3, in her attempt to show a teaching of implementing a translation lookaside buffer of reduced size. However, the Appellants do not see any disclosure by Hinton, of "implement[ing] a translation lookaside buffer of reduced size," since Hinton discloses a bit used to select from two different registers (i.e., physical register 0 (element 106) and physical register 1 (element 104)) located within a buffer (Hinton's translation write buffer (TWB)). Thus, Hinton does not teach or disclose "wherein using a single page frame number field implements a reduced size of a translation lookaside buffer," as recited in Claim 19. Examiner's reference to Hinton, using a physical register 0 (element 106) and a physical register 1 (element 104) at Col. 6, lines 55-58, does not teach what is recited in Claim 19. Therefore, the Examiner has not shown a teaching of Claim 19. Consequently, the Appellants request allowance of Claim 19.

G. Independent Claim 21

Claim 21 is directed to:

21. A method comprising:

obtaining a bit obtained from a virtual page number of a virtual address;

using said bit to determine which one of two storage registers will be used for:

a) writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and

a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, or

b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field.

The Appellants respectfully submit that the Examiner does not show a teaching of what is recited in Claim 21. The Examiner refers to translation write buffer (TWB) registers loaded with logical and physical addresses corresponding to two sets of logical and physical registers. Appellants would like to point out that the Examiner references Hinton, at col. 6, lines 37-67 by stating that **"Bit 12 selects which of the two entries in the TWB are to be used for this address."** In other words, the address is to be stored in either logical register 0 or logical register 1 of Hinton's translation write buffer (TWB). In comparison, Appellants' invention uses a bit "to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field," as recited in Claim 21. As stated by the Examiner, at page 7, lines 4-5 of the Office Action dated October 29, 2007, Hinton's invention "selects which of the two entries in a TWB are to be used for this address." Thus, Hinton's invention utilizes two entries as opposed to a single indexed entry; as a consequence, there is no teaching or disclosure of a "bit used to reduce size of said translation lookaside buffer by way of consolidating *two* page frame number fields

of said indexed entry into said *single* page frame number field," as recited in Claim 21 (emphasis denoted in italics). Therefore, the verbiage stated by the Examiner in the Office Action is not substantiated by Hinton. For example, the Examiner states "**[T]herefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field.**" From the preceding statement, the Examiner does not provide any logical reasoning as to how Hinton discloses or suggests "writing and reading even and odd page frame numbers into a single page frame number field." The Appellants do not see how referencing "an even or odd logical and physical address set" on a translation write buffer (TWB) has anything to do with "writing and reading even and odd page frame numbers into a single page frame number field." Thus, contrary to what the Office Action states, Hinton does not teach "a bit used to reduce size of said translation lookaside buffer" as recited in Claim 21. Therefore, the Office Action does not show a teaching of Claim 21. Appellants respectfully submit that the Examiner must show a teaching of each and every element / feature of Claim 21 if she wishes to maintain this rejection. Appellants respectfully submit that Claim 21 is in condition for allowance. Further, Appellants respectfully submit that Claims 22-28 are in condition for allowance for at least the reason that these claims depend on an allowable independent Claim 21. Therefore, Appellants request allowance of Claims 21-28.

H. Independent Claim 29

Claim 29 is directed to:

29. A method of performing a write operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in a data register;

assessing whether a value of said bit of a virtual page number is 0 or 1;

writing a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and

writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer.

With respect to Claim 29, the Examiner makes similar arguments that she made for Claims 12, 16, 18, and 21. Furthermore, the Examiner references the passages in Hinton that she previously used in her argument for Claims 12, 16, 18, and 21. Therefore, the Appellants request the Examiner to refer to Appellants' arguments made for Claims 12, 16, 18, and 21 in this Brief on Appeal. The Appellants respectfully submit that the Office Action does not show a teaching of what is recited in Claim 29. The Examiner alleges that "logical address bits" (per Hinton, at Col. 2, lines 9-10) corresponds to "Applicant's claimed page number." However, Appellants respectfully disagree because address bits do not teach a "page frame number field," as recited in Claim 29. Appellants respectfully submit that Claim 29 recites writing both "a first page

frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer." The Examiner has not shown a teaching of what is recited in the third and fourth clauses of Claim 29. For at least this reason, the Appellants respectfully submit that Claim 29 is in condition for allowance.

As was previously mentioned, the Examiner attempts to show a teaching of "to reduce the size of said translation lookaside buffer," by referencing Hinton, at Col. 6, lines 37-63 and Fig. 3; however, Hinton merely discloses *two* distinct and separate registers for storing "physical addresses." Hinton does not disclose a method "to reduce the size of a translation lookaside buffer." Thus, for at least this reason, the Appellants respectfully submit that Claim 29 is in condition for allowance.

Furthermore, the Examiner does not show a teaching of an "indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claim 29. The Appellants respectfully submit that Hinton discloses a bit which is simply used to select between two different registers (i.e., physical register 0 (element 106) and physical register 1 (element 104)) located within a buffer (Hinton's translation write buffer (TWB)). Thus, Hinton does not teach or disclose an "indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claim 29. Appellants respectfully submit that the Examiner has not shown a teaching of each and every

element recited in Claim 29. Appellants maintain that Claim 29 is in condition for allowance. Furthermore, dependent Claims 30-31 are in condition for allowance for at least the reason that they depend on allowable Claim 29.

I. Independent Claim 32

Claim 32 is directed to:

32. A method of performing a read operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer;

assessing whether a value of a bit of a virtual page number is 0 or 1;

reading a page frame number stored in a page frame number field of an indexed entry of said translation lookaside buffer;

storing said page frame number into a first register if said value is 0; and

storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer.

The Examiner has rejected Claim 32 by simply stating that "[The rationale in the rejection to claim 29 is herein incorporated]." Therefore, the Appellants request the Board to refer to Appellants' argument for Claim 29. Appellants respectfully submit that the Office Action does not show a teaching of each and every element recited in Claim 32. For example, the Examiner has not shown a teaching of "using a bit of a virtual page

number," as recited in Claim 32. For at least this reason, the Appellants respectfully submit that Claim 32 contains patentable subject matter. Furthermore, nowhere does Hinton teach an "indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claim 32. Therefore, Appellants maintain that Claim 32 is in condition for allowance. Furthermore, dependent Claim 33 is in condition for allowance for at least the reason that it depends on allowable Claim 32.

J. Independent Claim 34

Claim 34 is directed to:

34. A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising:

using a virtual page number stored in a first register;

comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer;

generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and

storing said identifying number into a second register.

Appellants respectfully submit that the Examiner does not show a teaching of "using a virtual page number stored in a first register," as recited in the first clause of

Claim 34. For at least this reason, the Appellants respectfully submit that Claim 34 contains patentable subject matter.

Appellants respectfully submit that the Examiner does not show a teaching of "comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer," as recited in the second clause of Claim 34. For at least this reason, the Appellants respectfully submit that Claim 34 contains patentable subject matter.

Appellants respectfully submit that the Examiner does not show a teaching of "generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number, and storing said identifying number into a second register," as recited in the third and fourth clauses of Claim 34.

The Examiner alleges that Hinton, at col. 5-6, lines 62-67 and 1-5; col. 1-2, lines 64-67 and 1-29; col. 6, lines 37-63; Figure 3; and col. 7, lines 5-14 teaches what is recited in Claim 34. The Examiner goes on to say:

> For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as

claimed by Applicant] [See figure 7 and related text].

Appellants respectfully submit that the statement "[t]herefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant" does not show a teaching of what is recited in Claim 34 because Claim 34 does not recite "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer." Instead, Claim 34 recites "using a virtual page number stored in a first register; comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register." Nowhere does Claim 34 recite "writing and reading even and odd page frame numbers ..." Therefore, the Appellants respectfully submit that the Examiner has not clearly shown a teaching of each and every element recited in Claim 34. Therefore, the rejection to Claim 34 should be reversed. For at least this reason, the Appellants respectfully submit that Claim 34 contains patentable subject matter. Appellants maintain that Claim 34 is in condition for allowance.

K. Independent Claim 41

Claim 41 is directed to:

41. A reduced size translation lookaside buffer comprising:

a virtual page number field used to store a virtual page number;

a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number.

The Examiner's argument for Claim 41 merely states "the rationale in the rejection to claim 21 is herein incorporated." As argued previously, the Appellants believe that the Examiner has been unable to show a teaching of what is recited in Claim 21. The Appellants respectfully submit that, among other things, the Examiner has not shown a teaching of Claim 41 since Claim 21 does not recite a "virtual page number field," as recited in the first clause of Claim 41. Furthermore, the Appellants respectfully submit that the Examiner does not show a teaching of "a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number." Based on what the Examiner states for Claim 21, the Examiner has not provided a logical argument that shows a teaching of Claim 41. Thus, for at least these reasons, Claim 41 contains patentable subject matter. Consequently, the Appellants request allowance of Claim 41. Furthermore, for at least the reason that Claims 42-43 depend on Claim 41, Claims 42-43 should be allowed as well.

II. REJECTION OF CLAIM 24 UNDER 35 U.S.C. § 103(a)

A. Dependent Claim 24

Claim 24 is directed to:

24. The method of Claim 23 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

The Examiner has rejected Claim 24 under 35 U.S.C. § 103(a) as being unpatentable over Hinton. The Examiner alleges that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs." Appellants respectfully submit that the Examiner does not provide a proper motivation to modify Hinton to incorporate "a MIPS control processor instruction set." Appellants do not see how "select[ing] from off the shelf processors at least to reduce cost and take advantage of existing system component designs" has anything to do with combining the teachings of Hinton with "a MIPS control processor instruction set," as recited in Claim 24. Therefore, the Appellants do not see how this statement is relevant to showing a teaching of Claim 24. In addition, Claim 24 is allowable for at least the reason that Claim 24 depends on an allowable Claim 23. Furthermore, Claim 24 is allowable for at least the reason that Claim 24 depends on an allowable independent Claim 21. Hence, for at least the foregoing reasons, Appellants submit that Claim 24 is in condition for allowance.

III. REJECTION OF CLAIMS 27 AND 28 UNDER 35 U.S.C. § 103(a)

A. Dependent Claim 27

Claim 27 is directed to:

27. The method of Claim 25 wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes.

Appellants respectfully disagree that it would have been obvious for one of ordinary skill in the art to "use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton." Furthermore, Appellants respectfully disagree that it would have been obvious to utilize a page mask size ranging from 4 kilobytes to 16 megabytes, as recited in Claim 27. The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the Examiner does not produce a prima facie case, the Appellant is under no obligation to submit evidence of unobviousness. Furthermore, the Examiner has not provided any suggestion or motivation, to support this conclusion. Therefore, for at least this reason, a prima facie case of obviousness has not been established. In addition, Claim 27 is allowable for at least the reason that Claim 27 depends on an allowable Claim 25. Furthermore, Claim 27 is allowable for at least the reason that Claim 27 depends on an allowable independent Claim 21. Hence, for at least the foregoing reasons, Appellants submit that Claim 27 is in condition for allowance.

B. Dependent Claim 28

Claim 28 is directed to:

28. The method of Claim 27 wherein said page mask size comprises 4 kilobytes.

Appellants respectfully disagree that it would have been obvious for one of ordinary skill in the art to "use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton." Furthermore, Appellants respectfully disagree that it would have been obvious to utilize a page mask size comprising 4 kilobytes, as recited in Claim 27. The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. Appellants feel that since the Examiner does not produce a prima facie case, the Appellant is under no obligation to submit evidence of unobviousness. Furthermore, the Examiner has not provided any suggestion or motivation, to support her conclusion. Therefore, for at least this reason, a prima facie case of obviousness has not been established, and a reversal of the rejection is requested. In addition, Claim 28 is allowable for at least the reason that Claim 28 depends on an allowable Claim 27. Furthermore, Claim 28 is allowable for at least the reason that Claim 28 depends on an allowable Claim 25. Also, Claim 28 is allowable for at least the reason that Claim 28 depends on an allowable independent Claim 21. Hence, for at least the foregoing reasons, Appellants submit that Claim 28 is in condition for allowance.

IV. REJECTION OF CLAIMS 35-38 AND 40 UNDER 35 U.S.C. § 103(a)

A. Independent Claim 35

Claim 35 is directed to:

35. A translation lookaside buffer system comprising:

a translation lookaside buffer;

a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field;

a second register used for storing a page size of said entry;

a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit;

a fourth register used for storing an even page frame number; and

a fifth register used for storing an odd page frame number, said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or said odd page frame number is to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer.

Appellants respectfully submit that the Examiner does not show a teaching of "said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or said odd page frame number is to be stored in said fifth register when performing a read operation, wherein

use of said single page frame number field reduces the size of said translation lookaside buffer," as recited in the sixth clause of Claim 35. For at least this reason, the Appellants respectfully submit that Claim 35 contains patentable subject matter.

While Claim 35 recites elements which differ from what is recited in Claim 29, the Examiner has given the same argument in Claim 35 that was presented for Claim 29. Therefore, for this reason alone, the Examiner has not shown a teaching of what is recited in Claim 35. However, the Appellants request the Board to consider Appellants' argument for Claim 29 with respect to a portion of the sixth clause of Claim 35. With respect to "wherein use of said single page frame number field reduces the size of said translation lookaside buffer," it appears that the Examiner attempts to show a teaching of "wherein use of said single page frame number field reduces the size of said translation lookaside buffer," by referencing Hinton, at Col. 6, lines 37-63 and Fig. 3; however, Hinton merely discloses *two* distinct and separate registers for storing "physical addresses." Hinton does not disclose a method "to reduce the size of a translation lookaside buffer." Thus, for at least this reason, the Appellants respectfully submit that Hinton does not teach "wherein use of said single page frame number field reduces the size of said translation lookaside buffer," as recited in the sixth clause of Claim 35. Therefore, for at least this reason, Claim 35 is in condition for allowance.

The Examiner references the same passages in Hinton as she did in Claim 29, in her attempt to show a teaching of what is recited in Claim 35. The Examiner references Hinton, at col. 2, lines 9-10; col. 6, lines 37-63; col. 7, lines 5-14; col. 7, lines 25-25 [sic]; Figure 7 and "related text"; col. 5-6, lines 62-67 and 1-5; col. 1-2, lines 64-67; and Figures 3 and 7 and "related text." However, none of these re-referenced passages teach

what is disclosed in the sixth clause of Claim 35. The Examiner has not shown a teaching of each and every element and/or feature recited in this sixth clause.

Hence, for at least the foregoing reasons, Appellants submit that Claim 35 is in condition for allowance. Furthermore, since Claims 36-38 and 40 depend on Claim 35, Claims 36-38 and 40 should be allowed as well.

B. Dependent Claim 37

Claim 37 is directed to:

37. The method of Claim 36 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

The Examiner has rejected Claim 37 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Hinton. The Examiner alleges that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs." Appellants respectfully submit that the Examiner does not provide a proper motivation to modify Hinton to incorporate "a MIPS control processor instruction set." Appellants do not see how "select[ing] from off the shelf processors at least to reduce cost and take advantage of existing system component designs" has anything to do with combining the teachings of Hinton with "a MIPS control processor instruction set," as recited in Claim 37.

Therefore, the Appellants do not see how this statement is relevant to showing a teaching of Claim 37. In addition, Claim 37 is allowable for at least the reason that Claim 37 depends on an allowable Claim 36. Furthermore, Claim 37 is allowable for at least the reason that Claim 37 depends on an allowable independent Claim 35. Hence, for at least the foregoing reasons, Appellants submit that Claim 37 is in condition for allowance.

CLAIMS APPENDIX

The following claims are involved in this appeal:

12. A method of improving the performance of address translation in a translation lookaside buffer comprising:

using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and

consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer.

13. The method of Claim 12 wherein said bit corresponds to the least significant bit of said virtual page number.

14. The method of Claim 12 wherein said address translation of said translation look aside buffer is performed by way of using a control processor instruction set.

15. The method of Claim 12 wherein said consolidating even and odd page frame number fields into said single page frame number field implements a translation lookaside buffer of reduced size.

16. A system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers.

17. The system of Claim 16 wherein said buffer comprises a translation lookaside buffer of reduced size.

18. A system to provide virtual to physical memory address translation of a translation lookaside buffer comprising:

a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer;

a first register for mapping an even page frame number to said single page frame number field; and

a second register for mapping an odd page frame number to said single page frame number field.

19. The system of Claim 18 wherein using a single page frame number field implements a reduced size of said translation lookaside buffer.

20. The system of Claim 19 wherein said virtual to physical memory address translation is performed by way of using TLB control processor instructions.

21. A method comprising:

obtaining a bit obtained from a virtual page number of a virtual address;

using said bit to determine which one of two storage registers will be used for:

a) writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, or

b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field.

22. The method of Claim 21 wherein said bit corresponds to the least significant bit of said virtual page number.

23. The method of Claim 21 wherein said reading and said writing is performed by way of using a translation lookaside buffer (TLB) control processor instruction set.

24. The method of Claim 23 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

25. The method of Claim 21 wherein said virtual address comprises 32 bits.

26. The method of Claim 25 wherein said virtual page number is specified by bits [31:12] of said virtual address.

27. The method of Claim 25 wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes.

28. The method of Claim 27 wherein said page mask size comprises 4 kilobytes.

29. A method of performing a write operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in a data register;

assessing whether a value of said bit of a virtual page number is 0 or 1;

writing a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and

writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer.

30. The method of Claim 29 wherein said bit corresponds to the least significant bit of said virtual page number.

31. The method of Claim 29 wherein a control processor is used to verify that said first page frame number and said second page frame number are valid.

32. A method of performing a read operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer;

assessing whether a value of a bit of a virtual page number is 0 or 1;

reading a page frame number stored in a page frame number field of an indexed entry of said translation lookaside buffer;

storing said page frame number into a first register if said value is 0; and

storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer.

33. The method of Claim 32 wherein said bit corresponds to the least significant bit of said virtual page number.

34. A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising:

using a virtual page number stored in a first register;

comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer;

generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and

storing said identifying number into a second register.

35. A translation lookaside buffer system comprising:

a translation lookaside buffer;

a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field;

a second register used for storing a page size of said entry;

a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit;

a fourth register used for storing an even page frame number; and

a fifth register used for storing an odd page frame number, said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or said odd page frame number is to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer.

36. The method of Claim 35 wherein said read and write operations are performed by way of using a translation lookaside buffer (TLB) control processor instruction set.

37. The method of Claim 36 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

38. The method of Claim 35 wherein said virtual page number is defined by a 32 bit virtual address.

39. The method of Claim 38 wherein said virtual page number is specified by bits [31:12] of said 32 bit virtual address.

40. The method of Claim 38 wherein said bit comprises the least significant bit (lsb) of said virtual page number.

41. A reduced size translation lookaside buffer comprising:

a virtual page number field used to store a virtual page number;

a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number.

42. The reduced size translation lookaside buffer of Claim 41 wherein said bit corresponds to the least significant bit of said virtual page number.

43. The reduced size translation lookaside buffer of Claim 41 wherein said virtual page number is defined by a 32 bit virtual address.

44. The reduced size translation lookaside buffer of Claim 41 wherein said virtual page number is specified by bits [31:12] of said 32 bit virtual address.

EVIDENCE APPENDIX
(37 C.F.R. § 41.37(c)(1)(ix))

Not applicable.

RELATED PROCEEDINGS APPENDIX
(37 C.F.R. § 41.37(c)(1)(x))

The Appellants are unaware of any related appeals or interferences.

CONCLUSION

For at least the foregoing reasons, the Appellants submit that Claims 12-44 are allowable in all respects. Reversal of the Examiner's rejections and issuance of a patent on the present Application are therefore requested from the Board.

PAYMENT OF FEES

The Commissioner is hereby authorized to charge $510 (to cover the Brief on Appeal Fee) and any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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